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The accordion imager, a new solid-state image sensor

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No image sensor can compete with the human eye. Even if a charge distribution could be produced in a solid-state image sensor with the same accuracy as an image is formed on the retina, the information could not be transferred in the same way. Each photosensitive element in the eye has its own channel for transferring the image information to the brain. A simulation of this system would require far too many connections. The information originating from all the individual image elements in solid-state image sensors is ultimately transferred through a single channel. The idea for the transfer of the image information in the 'accordion imager' described below was first put forward in the early eighties at Philips Research Laboratories.

Introduction

A solid-state image sensor seems to be an attractive alternative to the conventional television camera tube. In a camera tube an electron beam scans the charge distribution produced on a photoconductor by incident light. In most solid-state sensors the charge distribution is not scanned; the charge is transferred directly.

Major applications of such image sensors are to be found in monitoring and surveillance equipment, electronic cameras and even in toys. Because of the interesting applications in the consumer market it is important to keep the price of the imager low. Since the price is directly related to the size of the sensor, the sensor should be as small as possible without loss of resolution.

A solid-state image sensor has a number of advantages compared with a camera tube: it can be made in IC technology, its weight is low, it requires little power and it is small and robust. Image-lag or 'comet' effects can be avoided and the image area is not damaged if the light beam is too bright. The image quality, however, is not that of a camera tube. For a comparable image quality, a solid-state sensor should have a certain minimum number of picture elements (pixels). But this must not require any change in the critical dimensions (and hence a new technology) or make the chip too expensive. In the current state of the technology the chip will only compare with other image sensors if its area is less than 40 mm^2.

A solid-state image sensor is simply a silicon chip. It consists of two parts, an image section and a storage section. In the image section incident light generates electrons, which are collected in potential wells at defined positions on the surface (the pixels). This results in a distribution of charge packets that corresponds to an image. The size of a charge packet corresponds to the quantity of light that arrives at a pixel. After charge has been accumulated during a specific period (the 'integration period') this charge distribution is transferred in its entirety [1] to the storage section, which is shielded from light. The transfer has to be very fast to ensure that the charge packets in transit are not significantly affected by incident light. Nor, of

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[1] The charge distribution corresponding to an image is transferred in its entirety to the storage section situated below the image section. Sensors of this type are therefore called frame-transfer (FT) devices.

course, must there be any interaction between the charge packets. The potential wells in the silicon are produced by applying voltages to a number of electrodes positioned on the surface, perpendicular to linear channels of n-type silicon.

From the storage section the charge packets are transferred row by row (line by line) to the output register. Further processing for television pictures can then take place in the usual way.

The resolution of the sensor is determined by the number of pixels per unit area. The dimensions of a pixel are fixed by the width of one n-channel and by the number and dimensions of the electrodes that are necessary to produce the potential wells. In a four-phase image sensor a pixel comprises four electrodes (see *fig. 1*).

Fig. 2 shows a cross-section through part of a four-phase image sensor, which is essentially a shift register of the CCD type (charge-coupled device) [2]. A substrate of p-type silicon contains narrow channels of n-type material. Above this there is an insulating layer of silicon oxide, and on top of that layer there are the electrodes, consisting of polycrystalline silicon. Light passing through the electrodes and the insulating layer generates electrons in the silicon. In addition to electrons positive charge carriers are also generated, and these are conducted to earth. The potential wells in which the electrons are collected are created by applying a positive voltage to electrodes *2*, *3* and *4* and a negative voltage to electrodes *1*. The first signal (marked t_0) represents this situation, which remains unchanged for the full integration period of 20 ms. Then the charge distribution is transferred to the storage section. In the image sensor shown in fig. 2 this transfer is effected by generating a peristaltic 'potential movement' controlled by a clock signal. This propels the charge packets towards the storage section.

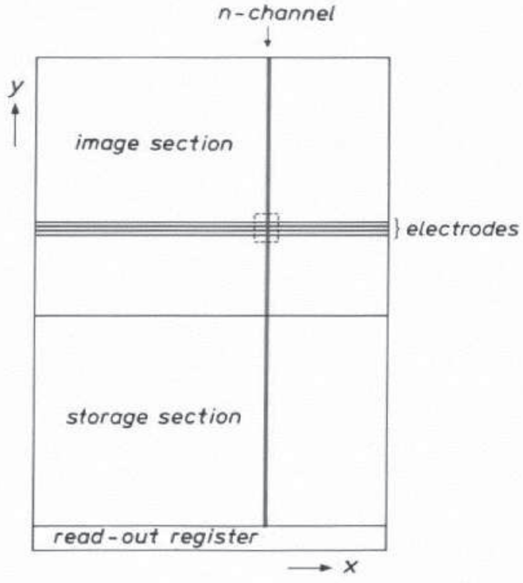

Fig. 1. Diagram representing a solid-state image sensor. From top to bottom, the sensor consists of three sections: an image section, a storage section and a read-out register. In the image and storage sections the n-channels are vertical (y-direction). For clarity only one n-channel is indicated. The electrodes run horizontally across the channels (x-direction). The figure shows only four electrodes for the image section. The dotted rectangle indicates a picture element (a pixel) in a four-phase image sensor. Each pixel contains a charge packet at the end of an integration period. After an integration period has been completed, all the charge packets are transferred to the storage section simultaneously. The storage section contains as many pixels as the image section. From the storage section the charge packets are moved towards the read-out register a row at a time. Each row of charge packets contains information that corresponds to a line in a television picture.

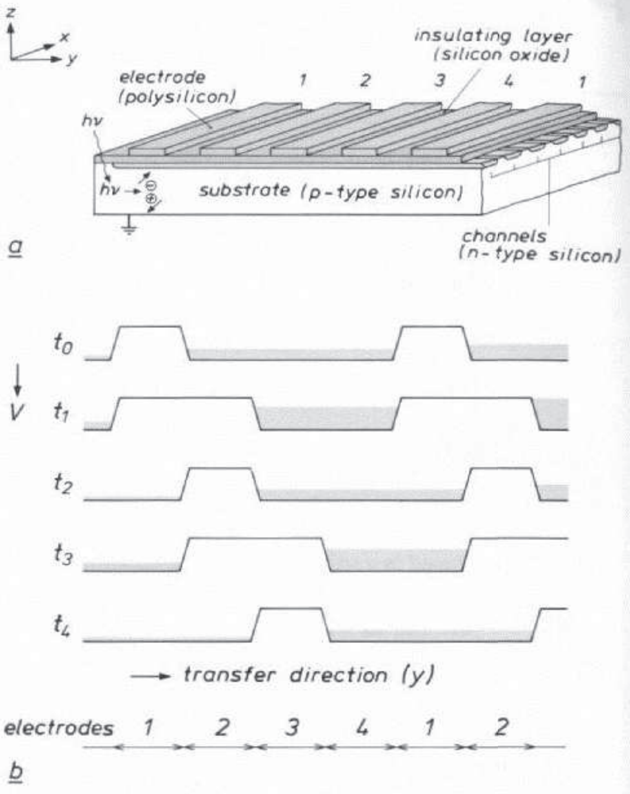

Fig. 2. *a*) Diagram of part of a four-phase solid-state image sensor. A p-type silicon substrate contains narrow channels of n-type silicon (in the y-direction). The surface of the substrate is covered with a layer of silicon oxide, and on top of that layer are the polysilicon electrodes (in the x-direction). The silicon oxide is necessary to prevent conduction between the substrate and the electrodes and between the electrodes themselves. Light passing through the transparent electrodes and the silicon oxide releases electrons and holes in the silicon ($h\nu \rightarrow +$ and $-$). The holes are conducted to earth and the electrons are collected in potential wells in the n-channels which are produced by applying voltages to the electrodes. *b*) Potential (V) in the silicon at consecutive times. The first signal represents the situation during an integration period. The electrons are collected in the potential well beneath the electrodes *2*, *3* and *4*. From the moment t_1 the changes in the voltages on the electrodes cause a peristaltic transfer of the charge packets. The blue colouring indicates the contents of a potential well. All the charge packets are transferred simultaneously.

The peristaltic 'potential movement' can in principle be produced with only three electrodes. We use four electrodes to obtain the usual interlacing for television pictures. During successive integration periods the voltage patterns on the electrodes are shifted symmetrically with respect to each other by an integer number of electrodes. In the field duration following the transfer in fig. 2, electrode *3* acts as a barrier electrode and the voltage on electrodes *1*, *2* and *4* produces the potential wells.

For the *collection* of the charge packets during the integration period two electrodes per pixel are sufficient. The peristaltic charge *transfer* can only take place if a pixel consists of more than two electrodes. In fig. 2 there are four. Because of these extra electrodes a row of pixels occupies a relatively large area on the chip. This has detrimental consequences for the resolution in the vertical direction (y), which is determined by the number of pixels per unit length. For this reason we wanted to make a sensor with smaller pixels. The obvious way of doing this is to make the electrodes narrower. However, this would require an entirely new technology for producing the sensors. Another way of making the pixels smaller is to reduce the number of electrodes in each row. This does not greatly affect the production process, but it does of course change the transfer mechanism. The way in which this problem has been solved in our new 'accordion imager' is treated in this article, which describes the operation of the sensor, its design and its characteristics.

The 'accordion' operation

The new 'accordion imager' [3] is a solid-state image sensor with only two electrodes per pixel, which serve alternately as integration and barrier electrodes in successive integration periods. The storage section also consists of elements with only two electrodes. Charge transfer takes place as follows. After an integration period the potential wells and barriers are doubled in width one at a time. This process starts at the interface between the image and storage sections of the sensor. The charge distribution is stretched like an accordion. When the lower edge of the storage section is reached the potential wells and barriers are reduced to a width of one electrode, one at a time. The charge distribution is now 'squeezed together' like an accordion. The result of this stretching and squeezing is that the entire charge distribution is moved from the image section to the storage section. The transfer from the storage section to the output register can be made in the same way.

It is clear that in this method of transfer the voltages on the electrodes will change in a more complex way than in the four-phase sensor. The benefits, however, are considerable: with the same technology as used for producing a four-phase sensor an equally large sensor can be made that has twice as many pixels, or a smaller sensor with the same number of pixels. The accordion imager has the same number of pixels as the four-phase sensor but occupies a smaller chip area.

The detailed action for the charge transfer in the accordion imager is illustrated in fig. 3 and fig. 4. At time t_0 (*fig. 3*) the sensor is in one of the two states in which charge is accumulated during a period of 20 ms, the integration period. At time t_1 the first charge packet (a) is stretched. At time t_2 it is pushed further towards the output. The other charge packets ($b, c, \ldots$) stay in position. At time t_3 the second charge packet (b) starts to move, and so on. This change from a static two-phase system to a dynamic four-phase system continues until every charge packet has been spread over two electrodes. The separation between each two charge packets has a width of two elec-

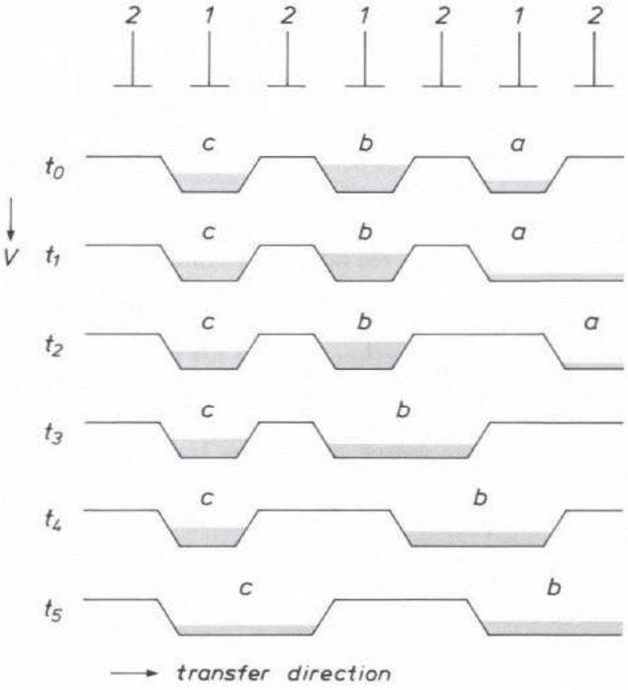

Fig. 3. Principle of the 'accordion' mechanism. The starting point is a two-phase system, in which charge is collected beneath the electrodes *1* during the integration period and the electrodes *2* form a barrier between the different charge packets. A four-phase system is built from this, a step at a time. The state at time t_0 occurs at the end of an integration period, t_1 to t_5 indicate the successive stages in 'stretching the accordion'. It can clearly be seen that charge packet a is transferred first, followed by charge packet b, and so on to the output of the sensor.

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[2] F. L. J. Sangster and K. Teer, Bucket-brigade electronics — new possibilities for delay, time-axis conversion, and scanning, IEEE J. SC-4, 131-136, 1969.

[3] The ideas on which this work is based were put forward by A. J. J. Boudewijns, now with the Consumer Electronics Division, Philips NPB, formerly with Philips Research Laboratories, and M. G. Collet and L. J. M. Esser of these laboratories.

trodes. At this moment the first packet has arrived at the first part of the storage section and the accordion starts to close up. The potential wells and barriers are gradually made one electrode wide.

The entire process of stretching and squeezing the 'accordion' is illustrated in *fig. 4* for a sensor in which the image and storage sections each have eight electrodes. Note that at the end of the cycle the sensor is in the appropriate state for collecting charge beneath the electrodes that were barrier electrodes in the previous integration period; this provides the interlacing.

In the accordion imager the charge transfer takes place over two times 588 electrodes (image and storage). This takes 0.5 ms, which is sufficiently short compared with the integration period of 20 ms. The application of the voltages to the electrodes is obviously more complicated than in the four-phase sensor. The voltage change is no longer the same for electrodes with the same number, as it was in the four-phase sensor. In the following section we shall show how the required voltage pattern on the electrodes is produced.

The accordion imager

Principle

So far we have considered the consequences of the changing voltages on the electrodes for the charge transfer. Let us now see how these voltage changes are produced.

The image sensor is controlled by two shift registers, one for the image section and one for the storage section. These shift registers consist of cells, each with a clock input. The output of each cell is connected to an electrode of the sensor and to the input of the next cell. At the input of the first cell the signal can be either *IM* (for the image section of the sensor) or *ST* (for the storage section of the sensor). The clock signals ϕ_1, which controls the clock inputs of the odd cells in each shift register, and ϕ_2, which controls the clock inputs of the even cells, make this input signal shift step by step through the register, with signal inversion after each cell. This process produces the required voltage pattern on the electrodes. The signal at the input of the first cell of the shift register (*IM* or *ST*) causes the stretching and squeezing of the accordion. The way in which this is done is illustrated in *fig. 5* for a small part of the sensor (8 electrodes of the image section and 8 electrodes of the storage section with the associated shift registers).

At the moment when the clock associated with a cell generates a pulse, the output of the cell takes on a value opposite to the value at the input. The input signals *IM* and *ST*, as shown in fig. 5*a*, produce the potential profile shown in fig. 5*b* on the electrodes $A_\text{I}, B_\text{I} \ldots$. As long as the input signal *IM* is changing, the potential wells and barriers are two electrodes wide and the charge packets are transferred. The variation of the potential wells and barriers with time can be seen in fig. 5 from the values of the outputs $A_\text{I}, B_\text{I}, \ldots$ at consecutive times. We see that the required potential pattern is produced at the numbered times, and that it corresponds to the state of the sensor as illustrated in fig. 4.

As soon as the input signal *IM* (or *ST*) becomes constant, the voltages on the electrodes of the image section (or storage section) also become constant, after a short delay. Gradually the accordion is squeezed shut, and the process continues until the potential distribution consists of wells and barriers, each with a width of only one electrode. This potential distribution remains unchanged as long as the signal *IM* remains constant. By keeping the input signal *IM* high in one integration period and low in the other, the electrodes function alternately as barrier and integration electrodes (see fig. 4 and fig. 5).

Correct operation of the sensor requires a number of synchronization signals — in addition to the clock signals ϕ_1 and ϕ_2 and the control signals *IM* and *ST*. These synchronization signals indicate the start and finish of the stretching of the two 'accordions' (the image and storage sections). They can be determined by counting the number of clock pulses, for example. Some of them can also be derived from the state of the shift register [4]. The first synchronization signal indicates the start of the stretching of the charge distribution in the image section and coincides with the end of the integration period. This signal must of course be supplied from outside the chip [5]. The end of the stretching process is reached when the potential of the final electrode of the image section, electrode H_I in the example given in figures 4 and 5, changes for the first time. The arrows in fig. 5 indicate the states from which the synchronization signals are derived. At this time, t_8, the accordion of the storage section starts to close up. There must then be no further change in the signal *ST*.

When the charge distribution in the storage section has completely closed up, signal *IM* is kept constant. The potential distribution in the image section also closes up. The time at which this must start to happen is reached when there is no further change in the potentials of the last two electrodes in the storage section (t_{15}).

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[4] A. J. P. Theuwissen, C. H. L. Weijtens and J. N. G. Cox, The accordion imager: more than just a CCD-sensor, Proc. Electronic Imaging 85, Boston 1985, pp. 87-90.

[5] J. N. G. Cox contributed to the design and construction of the special electronic units required here.

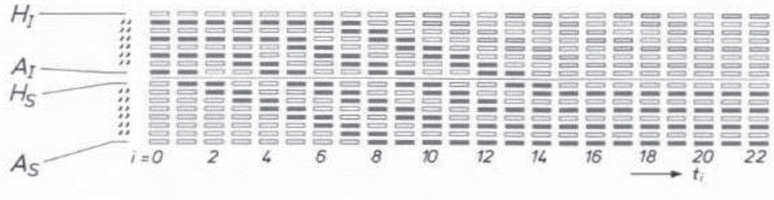

Fig. 4. A complete cycle of the stretching and squeezing of the 'accordion' of an image sensor consisting of 16 electrodes. A_I to H_I indicate the electrodes of the image section, A_s to H_s the electrodes of the storage section. A blue rectangle corresponds to an integration electrode that has a row of charge packets beneath it. A red rectangle corresponds to a barrier electrode, and a green rectangle to an electrode that has no charge beneath it yet, but is at a positive potential. The first column gives the potential distribution at t_0, i.e. at the time when a complete integration period has just finished. Beneath the electrodes A_I, C_I, E_I and G_I there are rows of charge packets (a, b, c and d). At t_1 the first row of charge packets starts to move, at t_3 the second, and so on. At time t_8 the first row of charge packets has arrived at the lower edge of the storage section, and the 'accordion' of the storage section can then be squeezed shut. At t_9 the first row of charge packets is again one electrode wide. We note that from t_9 the electrodes of the image section that no longer take part in the transfer of the current charge distribution take up a new potential distribution, which will collect charge during the next integration period. After the complete charge distribution has arrived in the storage section, a clock signal must be sent to provide the potential distribution in the image section with the required one-electrode-wide wells and barriers. From t_{21} charge can be collected beneath the electrodes (B_I, D_I, F_I and H_I). After completion of this integration period A_I, C_I, E_I and G_I are again used to collect the electrons, so that the complete cycle of stretching and squeezing starts again.

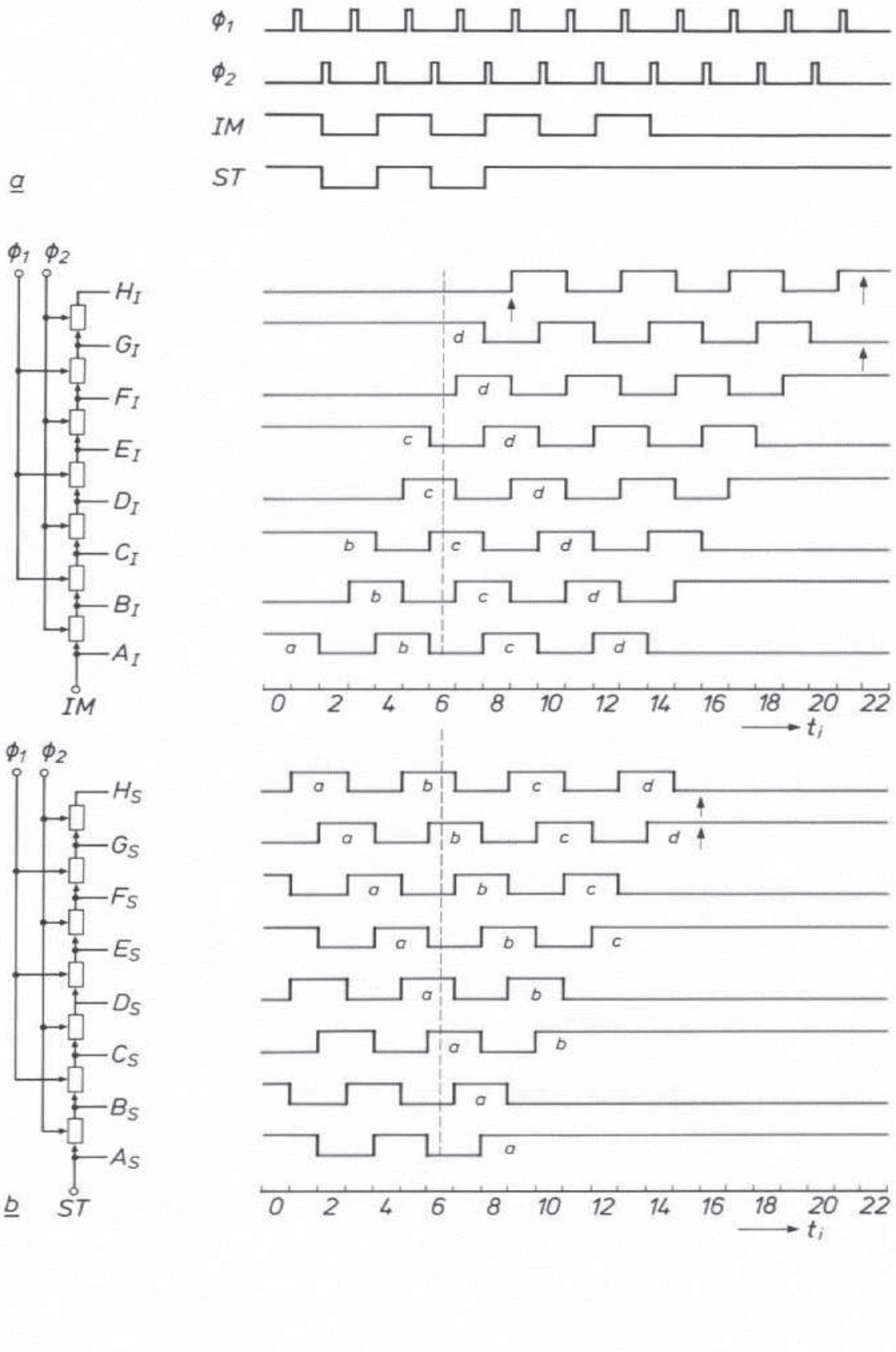

Fig. 5. *a*) Control signals for the transfer of the charge distribution from image section to storage section in the 16-electrode image sensor shown in fig. 4. *IM* and *ST* are the input signals of the 7-cell shift registers (shown as rectangles). These registers produce the potential profile shown in *b* on the electrodes A_s to H_I. The clock signals ϕ_1 and ϕ_2 are necessary for 'clocking' the input signal through the shift register. This potential profile causes the row of charge packets (whose position is indicated by a, b, c, ...) to be transferred from the image section to the storage section. The numbers below the time axis and the designations of the electrodes correspond to those given in fig. 4. At time t_6, for example (see dashed line), the potential pattern on the electrodes corresponds to the pattern in fig. 4 for t_6. The arrows indicate the points in the potential pattern from which the synchronization signals can be determined (see text). After the transfer the functions (separation and integration) of the electrodes in the image section are exchanged.

The final synchronization signal, which indicates that the accordion of the image section is squeezed fully shut, is derived from the states of the two final electrodes of the image section. For the sensor to function correctly it is not necessary to 'know' when the 'accordion' is squeezed shut again. However, to keep the dissipation low, the clocks are stopped at that time (t_{22}).

During the next integration period the charge distribution from the storage section is read out line by line (not shown in fig. 5). This is also done with the 'accordion' action. We should note that after this transfer the 'accordion' of the storage section is squeezed shut. This implies that at time t_0 the potential distribution on the electrodes of the storage section consists of wells and barriers two electrodes wide. At the end of this integration period a new charge distribution has been produced in the image section. At this moment the clocks are started again, and then the signals *IM* and *ST* are triggered by external pulses.

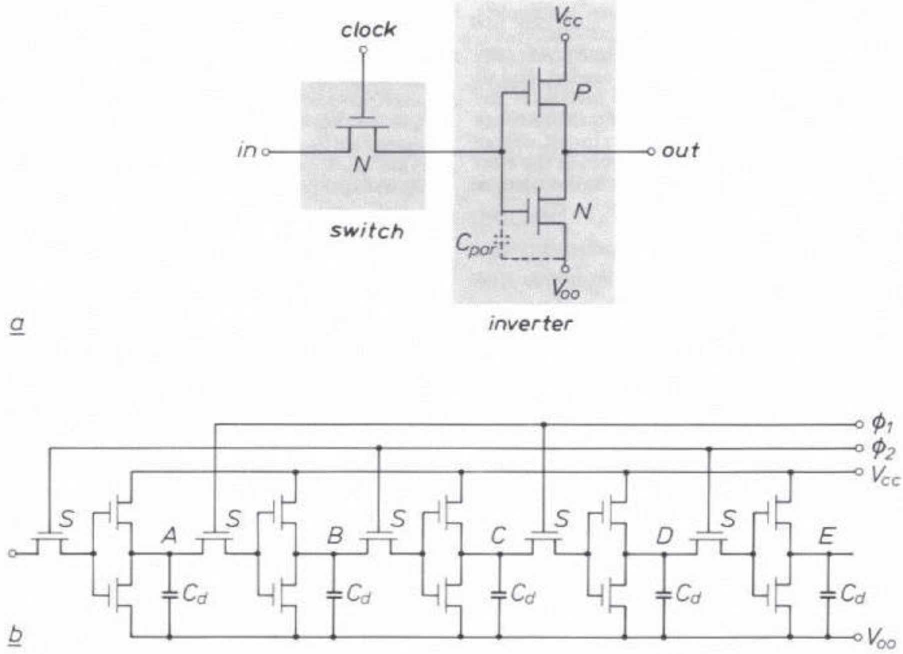

Fig. 6. *a*) Schematic diagram of a cell of the digital shift register that effects the transfer of the charge distribution. A cell consists of a combination of MOS transistors. The first NMOS transistor feeds the input signal along the register 'in phase with' the clock, which therefore acts as a switch. The output of this switch is connected to the gates of an NMOS transistor and a PMOS transistor. The source of the NMOS transistor is connected to a low voltage (V_{00}) and the source of the PMOS transistor is connected to a high (V_{cc}) voltage. This means that the drain electrodes, which are interconnected, are at a high voltage when the output of the switch — the value of the gate voltage — is low, or at a low voltage when the output of the switch is high. The final part of the cell acts as an inverter. The dashed capacitor C_{par} represents the parasitic capacitance of the connections. *b*) A row of these cells forms the shift register. The switches *S* are connected alternately to the clock signals ϕ_1 and ϕ_2. The output of each cell ($A_1, B_1, \ldots$) is connected to the input of the next one and to a CCD electrode (shown here as a capacitance C_d). The parasitic capacitances are not shown.

Practical design

The two shift registers for the control of the electrodes of the image and storage sections of the accordion imager have to be fabricated on the same chip as the CCD. The same design rules apply to the produc-

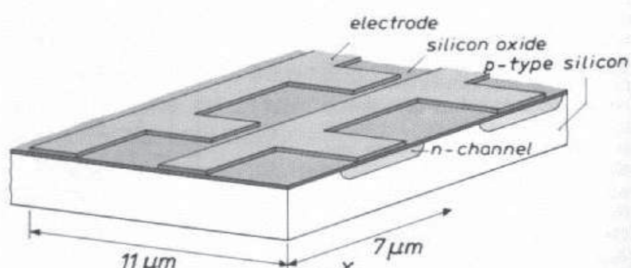

Fig. 7. Diagram showing the arrangement of the CCD electrodes and n-channels in the image section of the accordion imager. The electrodes are shaped in such a way that they do not cover the entire surface but leave some of the p-type material and a part of the n-channels accessible to incident light. This increases the blue sensitivity of the sensor. The polysilicon electrodes absorb light strongly in the blue wavelength range.

tion of the CCD and the shift registers. This means that the shift registers have to be fabricated in the 3.5-μm technology normally used for the CCDs. Moreover, the cells of the shift register should require as little energy as possible and occupy the smallest possible chip area. The simplest arrangement that delivers the required signal and also meets the above requirements is a combination of three MOS transistors per cell: two n-type and one p-type (see *fig. 6a*). The output signal from such a cell becomes the inverse of the input as soon as the clock gives a pulse. While the clock remains inactive (although the input may change) the output remains constant because of the stray capacitance of the inverter gate.

A shift register consists of 587 cells (the number of CCD electrodes less one). The inputs of the switches of these cells are connected alternately to one of the two clock signals. These two clock signals must not overlap in time. Otherwise, the shift register would behave like a row of unsynchronized inverters while both clocks were active.

Each CCD electrode is controlled by a cell of the shift register. The shift register obviously ought to be placed next to the electrodes on the chip, but this is not so easy.

The minimum dimensions of a photosensitive element of the image sensor are 7 μm in the horizontal direction and 11 μm in the vertical direction [6] (see *fig. 7*). The electrodes, which are made of polysilicon, are shaped in such a way that some of the p-type material and a part of the n-channels are accessible to incident light. This improves the sensitivity of the sensor to blue light (polysilicon is almost opaque to blue light). In the storage section of the sensor it is not necessary to leave a part of the silicon surface uncovered by the electrodes. The area of the part of the channel beneath the electrode must be the same as in the image section if it is to have the same charge storage capacity. This means that the dimension in the y-direction of a pixel in the storage section can be smaller than in the image section. This vertical dimension is 9 μm. In *fig. 8* it can indeed be seen that the storage section of the sensor is smaller than the image section.

It is obvious that a shift-register cell cannot be located next to every horizontal electrode: a cell consists of a number of p-n junctions and therefore has a vertical dimension several times the minimum width of 3.5 μm. For this reason a few of these cells (four) are placed side by side and on opposite sides of the CCD. The distribution of the available chip area among the different components can be seen in *Table I*.

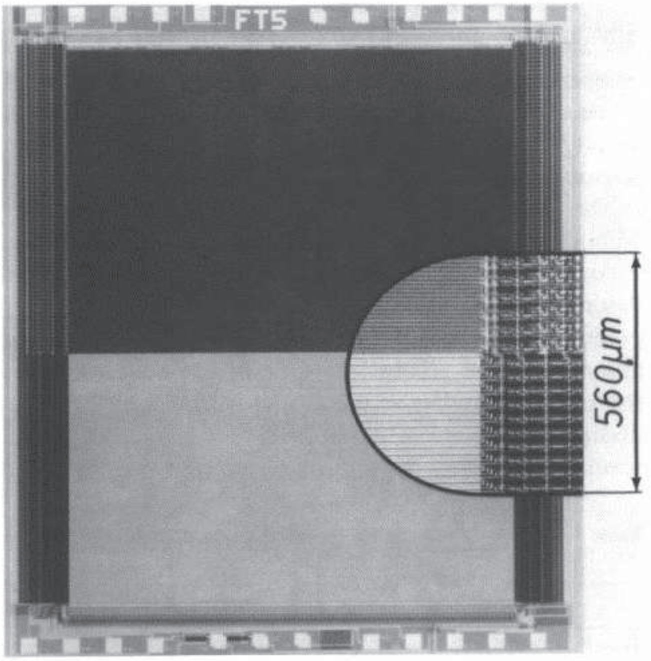

Fig. 8. The accordion imager. The storage section (the light region) is smaller than the image section (the dark region). The storage section is shielded from light by an aluminium layer. The n-channels are vertical, the CCD electrodes horizontal. On the left and right are the shift registers, which generate the voltages on the CCD electrodes. *Insert:* enlarged view of the transition from image section to storage section.

Table I. Allocation of the available chip space to the different sections of the sensor.

Section	Relative area
Image section	35.8%
Storage section	29.3%
CCD output register	2.9%
Digital shift registers	16.8%
Peripheral connections	15.2%

The synchronization signals that mark the start and finish of the stretching and closing of the 'accordions' (see previous subsection) can be determined by means of a small on-chip electronic circuit consisting of about 20 gates. This circuit determines the logical state of the final two electrodes of the image and storage sections. The clock signals and input signals are started or stopped depending on this state.

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[6] The minimum horizontal dimension follows from the 3.5-μm technology employed. The transfer in the horizontal direction takes place in a three-phase shift register. The length of a cell in this register, which really consists of three shift registers one above the other, is 21 μm. This is why the minimum dimension of an electrode of the shift register, and hence the minimum dimension of a channel, is 7 μm. The pixel matrix must have the standard TV format. This means that the ratio of the horizontal to the vertical dimensions of the image section must be 4:3. Since there are 604 pixels per line and 294 lines, a pixel must have a vertical dimension of 11 μm.

Characteristics of the sensor

To conclude, we shall recapitulate the characteristics of the accordion imager, and compare them with those of its predecessor, the four-phase image sensor. *Table II* gives the main characteristics of both types of sensor.

The area occupied by the accordion imager is only 56% of that of the four-phase device. This makes the accordion imager the smallest solid-state image sensor described in the literature with such a large number of pixels. This reduction of chip area has not entailed any sacrifice of resolution. One of the advantages of the smaller number of electrodes is that it reduces the dissipated power. A lower dissipated power per pixel results in a lower dark current, and therefore better image quality. Dark-current fluctuations, which are local, are one of the main limitations in the use of a solid-state image sensor. These fluctuations can cause bright spots to appear at various points in the picture.

Table II. Some characteristics of the accordion imager compared with those of the four-phase sensor.

	Four-phase sensor	Accordion imager
Type [1]	frame transfer	frame transfer
Chip area ($y \times x$)	9.41×7.01 $= 66\ \text{mm}^2$	7.01×5.45 $= 38.2\ \text{mm}^2$
Number of pixels ($y \times x$)	588×604	588×604
Pixel dimensions ($y \times x$)	$15.6 \times 10\ \mu\text{m}^2$	$11 \times 7\ \mu\text{m}^2$
Read-out rate	11.5 MHz	11.5 MHz
Layout rules	3.5 µm	3.5 µm
Number of electrodes per pixel	4	2

Another advantage is that the electronic control circuits not included on the chip are simpler and more compact. Less polysilicon is required on the chip, and this improves the photosensitivity of the sensor, particularly for blue light. The most important aspect of the accordion imager, however, is that a number of characteristics connected with the chip size and the number of pixels (especially the cost of the chip) are better than for other image sensors, yet it has not been necessary to design a completely new method of production or to develop an entirely new production process.

Summary. Solid-state image sensors are silicon chips in which a charge distribution is generated by incident light. The use of such devices in video cameras for the consumer market will depend greatly on the price of the sensor. As with all chips, this is closely dependent on the chip area. With a new read-out mechanism, in which the charge distribution is stretched out and squeezed shut like an accordion, it is possible to build an image sensor with two electrodes instead of the usual four for each line of the frame. The new sensor can be produced with the same technology as used for the four-phase sensor. The electronic control circuits can be fabricated on the chip with the sensor in a single process.